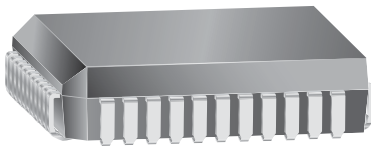


DMOS Dual Full-Bridge PWM Motor Driver

Features and Benefits

- ± 1.5 A, 50 V continuous output rating
- Low $r_{DS(on)}$ DMOS output drivers
- Programmable slow, fast, and mixed current-decay modes
- Serial-interface controls chip functions
- Synchronous rectification for low power dissipation
- Internal UVLO and thermal shutdown circuitry
- Crossover-current protection
- Sleep and idle modes

Package: 44-pin PLCC with internally fused pins (suffix ED)



Not to scale

Description

Designed for pulse width modulated (PWM) current control of two DC motors, the A3974 is capable of output currents to ± 1.5 A and operating voltages to 50 V. Internal fixed off-time PWM current-control timing circuitry can be programmed via a serial interface to operate in slow, fast, and mixed current-decay modes.

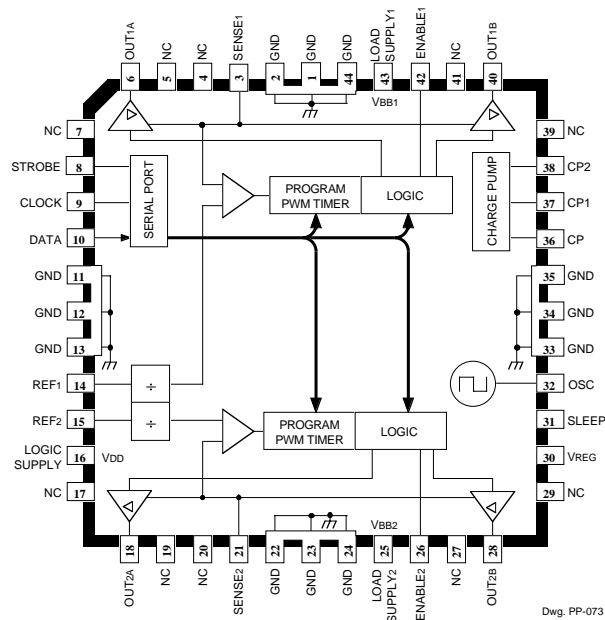
Independent ENABLE input terminals are provided for use in controlling the speed and torque of each DC motor with externally applied PWM control signals.

Synchronous rectification circuitry allows the load current to flow through the low $r_{DS(on)}$ of the DMOS output driver during the current decay. This feature will eliminate the need for external clamp diodes in most applications, saving cost and external component count, while minimizing power dissipation.

Internal circuit protection includes thermal shutdown with hysteresis, undervoltage monitoring of V_{DD} and the charge pump, and crossover-current protection. Special power-up sequencing is not required.

The A3974 is supplied in a 44-pin plastic PLCC with 3 internally fused pins on each side, for maximum heat dissipation. The fused pins are at ground potential and need no electrical isolation.

Pin-out Diagram



Selection Guide

| Part Number | Packing |
|--------------|---------------------|
| A3974SED-T | 27 pieces per tube |
| A3974SEDTR-T | 450 pieces per reel |

Absolute Maximum Ratings

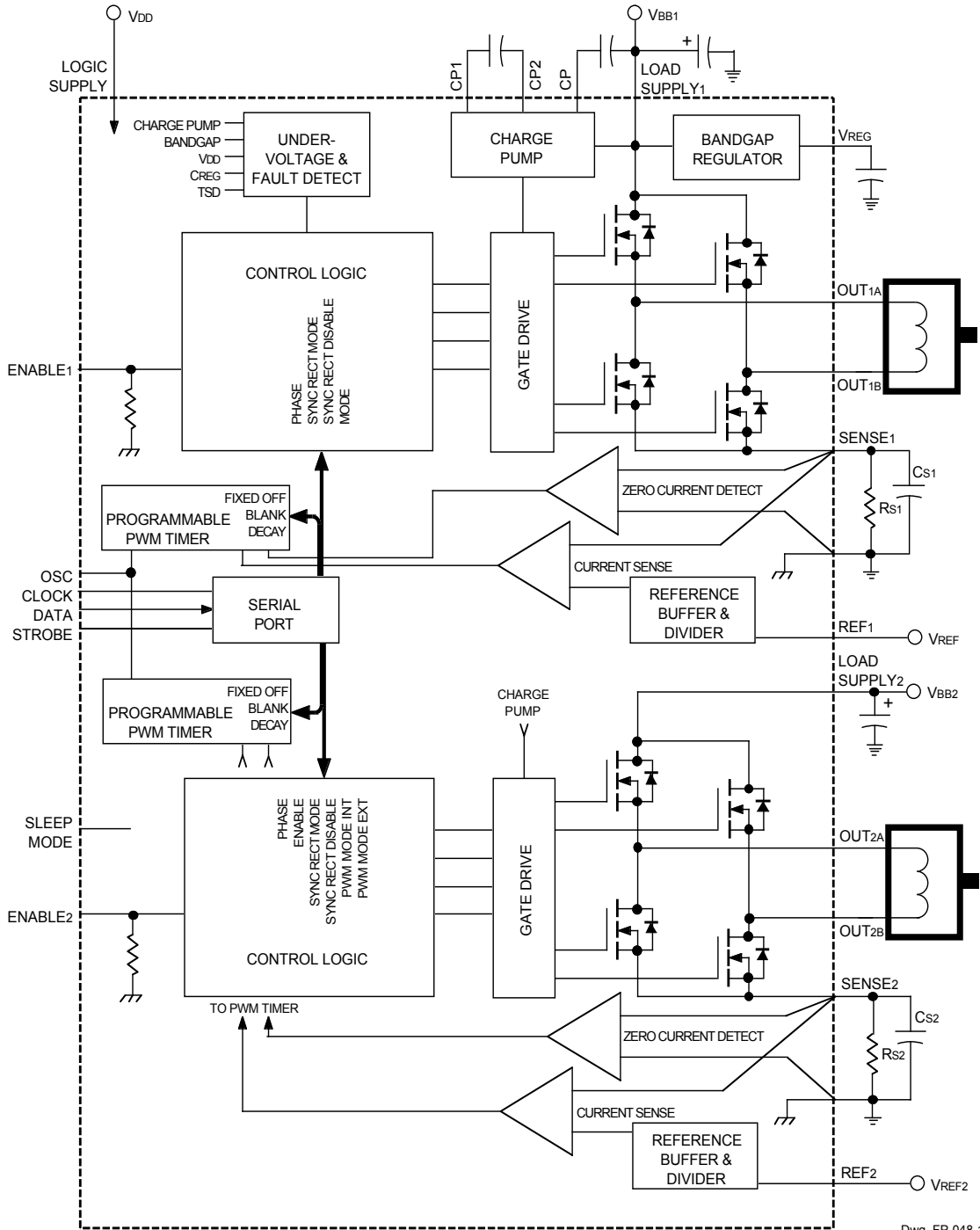
| Characteristic | Symbol | Notes | Rating | Units |
|-------------------------------|-------------------|--|--------------------------|-------|
| Load Supply Voltage | V_{BB} | | 50 | V |
| Logic Supply Voltage | V_{DD} | | 7.0 | V |
| Logic Input Voltage Range | V_{IN} | Continuous | -0.3 to $V_{DD} + 0.3$ | V |
| | | Pulsed, $t_w < 30$ ns | -1.0 to $V_{DD} + 1.0$ | V |
| Reference Voltage | V_{REF} | | 3 | V |
| Sense Voltage (DC) | V_S | Continuous | 0.5 | V |
| | | Pulsed, $t_w < 1$ μ s | 2.5 | V |
| Output Current | I_{OUT} | Output current rating may be limited by duty cycle, ambient temperature, and heat sinking. Under any set of conditions, do not exceed the specified current rating or a junction temperature of 150°C. | ± 1.5 | A |
| Operating Ambient Temperature | T_A | Range S | -20 to 85 | °C |
| Maximum Junction Temperature | $T_J(\text{max})$ | | 150 | °C |
| Storage Temperature | T_{stg} | | -55 to 150 | °C |

Thermal Characteristics may require derating at maximum conditions, see application information

| Characteristic | Symbol | Test Conditions* | Value | Units |
|----------------------------|-----------------|-------------------------------------|-------|-------|
| Package Thermal Resistance | $R_{\theta JA}$ | 4-layer PCB based on JEDEC standard | 22 | °C/W |
| | $R_{\theta JT}$ | | 6 | °C/W |

*Additional thermal information available on the Allegro website.

FUNCTIONAL BLOCK DIAGRAM



Dwg. FP-048-1

ELECTRICAL CHARACTERISTICS at $T_A = +25^\circ\text{C}$, $V_{BB} = 50\text{ V}$, $V_{DD} = 5.0\text{ V}$, $f_{\text{PWM}} < 50\text{ kHz}$ (unless otherwise noted).

| Characteristic | Symbol | Test Conditions | Limits | | | Units |
|--|-----------------|--|--------|-------|----------|---------------|
| | | | Min. | Typ. | Max. | |
| Output Drivers | | | | | | |
| Load Supply Voltage Range | V_{BB} | Operating | 15 | — | 50 | V |
| | | During sleep mode | 0 | — | 50 | V |
| Output Leakage Current | I_{DSS} | $V_{OUT} = V_{BB}$ | — | <1.0 | 20 | μA |
| | | $V_{OUT} = 0\text{ V}$ | — | <-1.0 | -20 | μA |
| Output ON Resistance | $r_{DS(on)}$ | Source driver, $I_{OUT} = -1.5\text{ A}$ | — | 0.5 | 0.55 | Ω |
| | | Sink driver, $I_{OUT} = 1.5\text{ A}$ | — | 0.315 | 0.35 | Ω |
| Body Diode Forward Voltage | V_F | Source diode, $I_F = 1.5\text{ A}$ | — | — | 1.2 | V |
| | | Sink diode, $I_F = 1.5\text{ A}$ | — | — | 1.2 | V |
| Load Supply Current | I_{BB} | $f_{\text{PWM}} < 50\text{ kHz}$ | — | 4.0 | 7.0 | mA |
| | | Charge pump on, outputs disabled | — | 2.0 | 5.0 | mA |
| | | Sleep or idle mode | — | — | 20 | μA |
| Control Logic | | | | | | |
| Logic Supply Voltage Range | V_{DD} | Operating | 4.5 | 5.0 | 5.5 | V |
| Logic Input Voltage | $V_{IN(1)}$ | | 2.0 | — | — | V |
| | $V_{IN(0)}$ | | — | — | 0.8 | V |
| Logic Input Current (except ENABLE) | $I_{IN(1)}$ | $V_{IN} = 2.0\text{ V}$ | — | <1.0 | ± 20 | μA |
| | $I_{IN(0)}$ | $V_{IN} = 0.8\text{ V}$ | — | <1.0 | ± 20 | μA |
| ENABLE Input Current | $I_{EN(1)}$ | $V_{EN} = 2.0\text{ V}$ | — | 40 | 100 | μA |
| | $I_{EN(0)}$ | $V_{EN} = 0.8\text{ V}$ | — | 16 | 30 | μA |
| OSC Input Frequency | f_{OSC} | | 2.9 | — | 6.1 | MHz |
| OSC Input Duty Cycle | — | | 40 | — | 60 | % |
| OSC Input Hysteresis | ΔV_{IN} | | 200 | — | 400 | mV |
| Reference Input Voltage Range | V_{REF} | Operating | 0 | — | 2.6 | V |

continued next page ...

ELECTRICAL CHARACTERISTICS at $T_A = +25^\circ\text{C}$, $V_{BB} = 50\text{ V}$, $V_{DD} = 5.0\text{ V}$, $f_{\text{PWM}} < 50\text{ kHz}$ (unless otherwise noted), continued.

| Characteristic | Symbol | Test Conditions | Limits | | | Units |
|----------------------------------|--------------------------|---|--------|----------|-----------|------------------|
| | | | Min. | Typ. | Max. | |
| Control Logic (continued) | | | | | | |
| Reference Input Current | I_{REF} | $V_{\text{REF}} = 2.6\text{ V}$ | — | — | ± 1.0 | μA |
| Reference Input Offset Voltage | V_{IO} | | — | ± 10 | — | mV |
| Reference Divider Ratio | V_{REF}/V_S | D16 = 1 | — | 10 | — | — |
| | | D16 = 0 | — | 5.0 | — | — |
| Gain (G_m) Error (note 3) | E_G | $V_{\text{REF}} = 2.6\text{ V}$, D16 = 0 | — | 0 | ± 4.0 | % |
| | | $V_{\text{REF}} = 0.5\text{ V}$, D16 = 0 | — | 0 | ± 14 | % |
| | | $V_{\text{REF}} = 2.6\text{ V}$, D16 = 1 | — | 0 | ± 4.0 | % |
| | | $V_{\text{REF}} = 0.5\text{ V}$, D16 = 1 | — | 0 | ± 10 | % |
| Propagation Delay Time | t_{pd} | 50% TO 90%: PWM change to source on | 600 | 750 | 1000 | ns |
| | | PWM change to source off | 50 | 150 | 350 | ns |
| | | PWM change to sink on | 600 | 750 | 1000 | ns |
| | | PWM change to sink off | 50 | 150 | 350 | ns |
| Crossover Delay Time | t_{COD} | SR enabled | 300 | 600 | 1000 | ns |
| Thermal Shutdown Temperature | T_J | | — | 165 | — | $^\circ\text{C}$ |
| Thermal Shutdown Hysteresis | ΔT_J | | — | 15 | — | $^\circ\text{C}$ |
| UVLO Enable Threshold | V_{UVLO} | Increasing V_{DD} | 3.9 | 4.2 | 4.45 | V |
| UVLO Hysteresis | ΔV_{UVLO} | | 0.05 | 0.10 | — | V |
| Logic Supply Current | I_{DD} | $f_{\text{PWM}} < 50\text{ kHz}$ | — | — | 10 | mA |
| | | Outputs off | — | — | 8.0 | mA |
| | | Idle mode (D18 = 1, D19 = 0) | — | — | 1.5 | mA |
| | | Sleep mode (inputs below 0.5 V) | — | — | 100 | μA |

- NOTES: 1. Typical Data is for design information only.
 2. Negative current is defined as coming out of (sourcing) the specified device terminal.
 3. $E_G = [(V_{\text{REF}}/\text{Range}) - V_S]/(V_{\text{REF}}/\text{Range})$.

FUNCTIONAL DESCRIPTION

Serial Interface. The A3974SED is controlled via a 3-wire (clock, data, strobe) serial port. The programmable functions allow maximum flexibility in configuring the PWM to the motor drive requirements. The serial data is written as two 20-bit words: 1 bit to select the word and 19 bits of data. The data is clocked in starting with D19.

Word 0 Bit Assignments

| Select Word 0 (D18 = 0) | |
|-------------------------|----------------------------------|
| Bit | Function |
| D0 | Bridge 1 blank time LSB |
| D1 | Bridge 1 blank time MSB |
| D2 | Bridge 1 off-time LSB |
| D3 | Bridge 1 off-time bit 1 |
| D4 | Bridge 1 off-time bit 2 |
| D5 | Bridge 1 off-time bit 3 |
| D6 | Bridge 1 off-time MSB |
| D7 | Bridge 1 fast-decay time bit LSB |
| D8 | Bridge 1 fast-decay time bit 1 |
| D9 | Bridge 1 fast-decay time bit 2 |
| D10 | Bridge 1 fast-decay time MSB |
| D11 | Bridge 1 sync. rect. control |
| D12 | Bridge 1 sync. rect. control |
| D13 | Bridge 1 external PWM mode |
| D14 | Bridge 1 enable |
| D15 | Bridge 1 phase |
| D16 | Bridge 1 reference range select |
| D17 | Bridge 1 internal PWM mode |
| D18 | Word select = 0 |
| D19 | Test mode |

D0 – D1 Blank Time. The current-sense comparator is blanked when any output driver is switched on, according to the table below. f_{osc} is the oscillator input frequency.

| D1 | D0 | Blank Time |
|----|----|--------------|
| 0 | 0 | $4/f_{osc}$ |
| 0 | 1 | $6/f_{osc}$ |
| 1 | 0 | $12/f_{osc}$ |
| 1 | 1 | $24/f_{osc}$ |

D2 – D6 Fixed Off Time. This five-bit word sets the fixed off-time for the internal PWM control circuitry. The off-time is defined by

$$t_{off} = (8 [1 + N]/f_{osc}) - 1/f_{osc}$$

where $N = 0 \dots 31$

For example, with an oscillator frequency of 4 MHz, the fixed off-time will be adjustable from 1.75 μ s to 63.75 μ s in increments of 2 μ s.

D7 – D10 Fast Decay Time. This four-bit word sets the fast-decay portion of the fixed off-time for the internal PWM control circuitry. This will only have impact if mixed-decay mode is selected (via bit D17). For $t_{fd} > t_{off}$, the device will effectively operate in fast-decay mode. The fast-decay portion is defined by

$$t_{fd} = (8[1 + N]/f_{osc}) - 1/f_{osc}$$

where $N = 0 \dots 15$

For example, with an oscillator frequency of 4 MHz, the fast-decay time will be adjustable from 1.75 μ s to 31.75 μ s in increments of 2 μ s.

D11 – D12 Synchronous Rectification.

| D12 | D11 | Synchronous Rectifier |
|-----|-----|-----------------------|
| 0 | 0 | Disabled |
| 0 | 1 | Low side only |
| 1 | 0 | Active |
| 1 | 1 | Passive |

The different modes of operation are described in the synchronous rectification section of the functional description.

D13 External PWM Decay Mode. This bit determines the current-decay mode when using ENABLE chopping for external PWM current control.

| D13 | Mode |
|-----|------|
| 0 | Fast |
| 1 | Slow |

continued next page ...

FUNCTIONAL DESCRIPTION (continued)

D14 Enable Logic. This bit, in conjunction with ENABLE, determines if the output drivers are in the chopped or on state.

| ENABLE1 | D14 | Mode |
|---------|-----|---------|
| 0 | 0 | Chopped |
| 1 | 0 | On |
| 0 | 1 | On |
| 1 | 1 | Chopped |

D15 Phase Logic. This bit determines if the device is operating in the forward or reverse state.

| D15 | State | OUT _A | OUT _B |
|-----|---------|------------------|------------------|
| 0 | Reverse | L | H |
| 1 | Forward | H | L |

D16 G_m Range Select. This bit determines if V_{REF} is divided by 5 or 10.

| D16 | Divider |
|-----|---------|
| 0 | ÷10 |
| 1 | ÷5 |

D17 Bridge 2 Mode. This bit determines slow or mixed decay for internal current-control operation.

| D17 | Decay Mode |
|-----|------------|
| 0 | Mixed |
| 1 | Slow |

D19 Test Mode. This bit is reserved for testing and should never be changed by the user. Default (low) operates the device in normal mode.

Word 1 Bit Assignments

| Select Word 1 (D18 = 1) | |
|-------------------------|----------------------------------|
| Bit | Function |
| D0 | Bridge 2 blank time LSB |
| D1 | Bridge 2 blank time MSB |
| D2 | Bridge 2 off-time LSB |
| D3 | Bridge 2 off-time bit 1 |
| D4 | Bridge 2 off-time bit 2 |
| D5 | Bridge 2 off-time bit 3 |
| D6 | Bridge 2 off-time MSB |
| D7 | Bridge 2 fast-decay time bit LSB |
| D8 | Bridge 2 fast-decay time bit 1 |
| D9 | Bridge 2 fast-decay time bit 2 |
| D10 | Bridge 2 fast-decay time bit MSB |
| D11 | Bridge 2 sync. rect. control |
| D12 | Bridge 2 sync. rect. control |
| D13 | Bridge 2 external PWM mode |
| D14 | Bridge 2 enable |
| D15 | Bridge 2 phase |
| D16 | Bridge 2 reference range select |
| D17 | Bridge 2 internal PWM mode |
| D18 | Word select = 1 |
| D19 | Idle mode |

D0 - D17. Identical definitions as Word 0, with Word 1 selected. Data is written to Full Bridge 2.

D19 Idle Mode. The device can be placed in a low-power “idle” mode by writing a “0” to D19. The outputs will be disabled, the charge pump will be turned off, and the device will draw a lower load supply current. The undervoltage monitor circuit will remain active. D19 should be programmed high for 1 ms before attempting to enable any output driver.

continued next page ...

FUNCTIONAL DESCRIPTION (continued)

V_{REG}. This internally generated supply voltage is used to operate the sink-side DMOS outputs. V_{REG} is internally monitored and in the case of a fault condition, the outputs of the device are disabled. The V_{REG} terminal should be decoupled with a 0.22 μF capacitor to ground.

Charge Pump. The charge pump is used to generate a supply voltage greater than V_{BB} to drive the source-side DMOS gates. A 0.22 μF ceramic capacitor should be connected between CP1 and CP2 for pumping purposes. A 0.22 μF ceramic capacitor should be connected between V_{CP} and V_{BB} to act as a reservoir to run the high-side DMOS devices. The CP voltage is internally monitored and in the case of a fault condition, the outputs of the device are disabled.

Shutdown. In the event of a fault due to excessive junction temperature, or low voltage on CP or V_{REG}, the outputs of the device are disabled until the fault condition is removed. At power up, or in the event of low V_{DD}, the UVLO circuit disables the drivers and resets the data in the serial port to all zeros.

Current Regulation. Load current is regulated by an internal fixed off-time PWM control circuit. When the outputs of the DMOS H-bridge are turned on, the current increases in the motor winding until it reaches a trip value determined by the external sense resistor (R_S), the applied analog reference voltage (V_{REF}), and serial data bit D16:

$$\text{When D16} = 0 \dots\dots\dots I_{\text{TRIP}} = V_{\text{REF}}/10R_{\text{S}}$$

$$\text{When D16} = 1 \dots\dots\dots I_{\text{TRIP}} = V_{\text{REF}}/5R_{\text{S}}$$

At the trip point, the sense comparator resets the source-enable latch, turning off the source driver (except in the case of low-side only mode where the sink driver is turned off). The load inductance then causes the current to recirculate for the serial-port programmed fixed off-time period. The current path during recirculation is determined by the configuration of slow/mixed-decay mode (D17) and the synchronous rectification control bits (D11 and D12).

Sleep Mode. The input terminal SLEEP is dedicated to putting the device into a minimum current draw mode. When asserted

low, the serial port will be reset to all zeros and all circuits will be disabled.

PWM Timer Function. The PWM timer is programmable via the serial port (bits D2 – D10) to provide fixed off-time PWM signals to the control circuitry. In mixed current-decay mode, the first portion of the off time operates in fast decay, until the fast-decay time count is reached (serial bits D7 – D10), followed by slow decay for the rest of the off-time period (bits D2 – D6). If the fast-decay time is set longer than the off-time, the device effectively operates in fast-decay mode. Bit D17 selects mixed or slow decay.

Synchronous Rectification. When a PWM off cycle is triggered, either by an ENABLE chop command or internal fixed off-time cycle, load current will recirculate according to the decay mode selected by the control logic. After a short crossover delay, the A3974 synchronous rectification feature will turn on the appropriate MOSFET (or pair of MOSFETs for the mixed decay portion of the off-time) during the current decay and effectively short out the body diodes with the low I_{DS(on)} driver. This will lower power dissipation significantly and can eliminate the need for external Schottky diodes.

Synchronous rectification can be configured in active mode, passive mode, low side only, or disabled via the serial port (bits D11 and D12). The active mode prevents reversal of load current by turning off synchronous rectification when a zero current level is detected. Passive mode will allow reversal of current but will turn off the synchronous rectifier circuit if the load current inversion ramps up to the current limit set by V_{REF}/10R_S (when D16 = 0) or V_{REF}/5R_S (when D16 = 1).

Low side only mode will switch the low-side MOSFETs on during the off time to short out the current path through the MOSFET body diode. With this setting, the high-side MOSFETs will not synchronously rectify so four external diodes from output to supply are recommended. This mode is intended for use with high-power applications where it is desired to save the expense of two external diodes per bridge. In this mode, the sink-side MOSFETs are chopped during the PWM off time. In all other cases, the source-side MOSFETs are chopped in response to a PWM OFF command.

APPLICATIONS INFORMATION

Current Sensing. To minimize inaccuracies in sensing the I_{TRIP} current level caused by ground-trace IR drops, the sense resistor should have an independent ground return to a ground terminal of the device. For low-value sense resistors, the IR drops in the PCB sense traces of the resistor can be significant and should be taken into account. The use of sockets should be avoided as they can introduce variation in R_S due to their contact resistance.

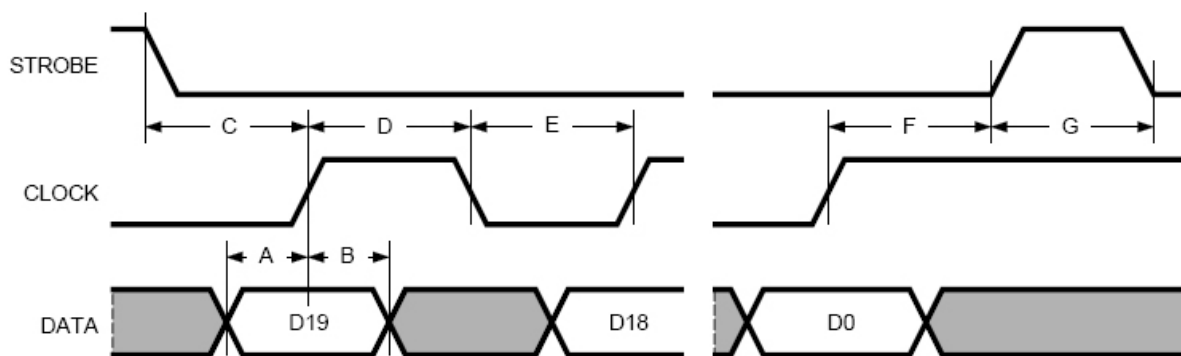
The maximum value of R_S is given as $R_S = 0.5/I_{TRIPMAX}$.

Braking. The braking function is implemented by driving the device in slow-decay mode via serial port bit D13, enabling synchronous rectification via bits D11 and D12, and applying an enable chop command with the combination of D14 and the ENABLE input terminal. Because it is possible to drive current in both directions through the DMOS switches, this configuration effectively shorts out the motor-generated BEMF as long as the ENABLE chop mode is asserted. It is important to note that the internal PWM current-control circuit will not limit the current when braking, because the current does not flow through the sense resistor. The maximum brake current can be approximated by V_{BEMF}/R_L . Care should be taken to ensure that the maximum ratings of the device are not exceeded in worst-case braking situations of high speed and high inertial loads.

Thermal protection. Circuitry turns off all drivers when the junction temperature reaches 165°C typically. It is intended only to protect the device from failures due to excessive junction temperatures and should not imply that output short circuits are permitted. Thermal shutdown has a hysteresis of approximately 15°C.

Layout. The printed wiring board should use a heavy ground plane. For optimum electrical and thermal performance, the driver should be soldered directly onto the board. The ground side of R_S should have an individual path to a ground terminal of the device. This path should be as short as is possible physically and should not have any other components connected to it. The load supply terminal, V_{BB} , should be decoupled with an electrolytic capacitor (>47 μF is recommended) placed as close to the device as is possible.

Serial Port Write Timing Operation. Data is clocked into shift register on the rising edge of CLOCK signal. Normally, STROBE will be held high, and only will be brought low to initiate a write cycle. Refer to diagram below and specification table for timing requirements.



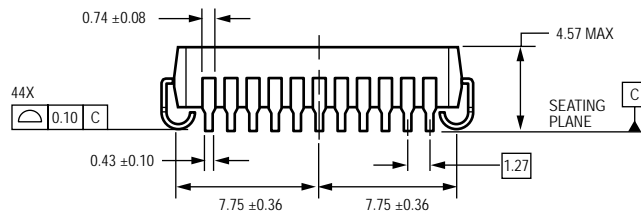
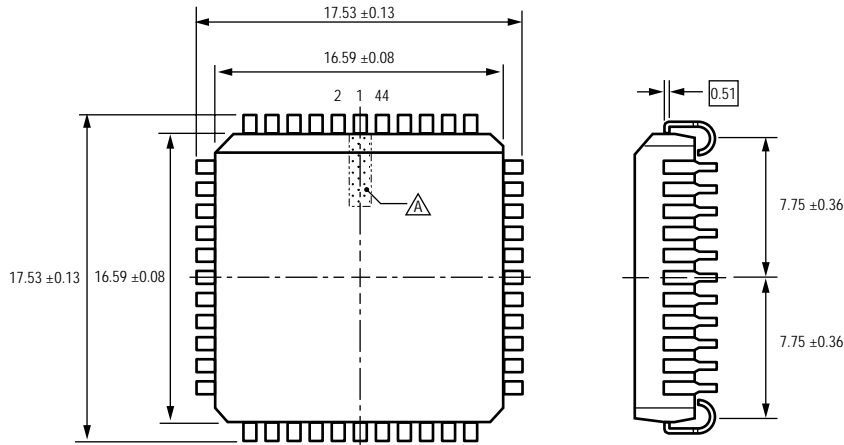
Dwg. WP-038

| | |
|--|-------|
| A. Minimum Data Setup Time | 15 ns |
| B. Minimum Data Hold Time..... | 10 ns |
| C. Minimum Setup Strobe to Clock Rising Edge | 50 ns |
| D. Minimum Clock High Pulse Width | 50 ns |
| E. Minimum Clock Low Pulse Width | 50 ns |
| F. Minimum Setup Clock Rising Edge to Strobe | 50 ns |
| G. Minimum Strobe Pulse Width | 50 ns |

Terminal List

| Terminal Name | Terminal Description | Terminal Number |
|--------------------------|--|------------------------|
| GND | Power and logic ground terminals | 1, 2 |
| SENSE ₁ | Sense resistor terminal for bridge 1 | 3 |
| NC | No (internal) connection | 4, 5 |
| OUT _{1A} | DMOS H-bridge 1 – output A | 6 |
| NC | No (internal) connection | 7 |
| STROBE | Logic input for serial Interface | 8 |
| CLOCK | Logic input for serial Interface | 9 |
| DATA | Logic input for serial Interface | 10 |
| GND | Power and logic ground terminals | 11, 12, 13 |
| REF ₁ | G _m reference input voltage – bridge 1 | 14 |
| REF ₂ | G _m reference input voltage – bridge 2 | 15 |
| LOGIC SUPPLY | V _{DD} , the low voltage (typically 5 V) supply | 16 |
| NC | No (internal) connection | 17 |
| OUT _{2A} | DMOS H-bridge 2 – output A | 18 |
| NC | No (internal) connection | 19, 20 |
| SENSE ₂ | Sense resistor pin for bridge 2 | 21 |
| GND | Power and logic ground terminals | 22, 23, 24 |
| LOAD SUPPLY ₂ | V _{BB2} , the high current, 20 V to 50 V, supply for bridge 2 | 25 |
| ENABLE ₂ | Logic input for bridge 2 – enable control | 26 |
| NC | No (internal) connection | 27 |
| OUT _{2B} | DMOS H-bridge 2 – output B | 28 |
| NC | No (internal) connection | 29 |
| V _{REG} | Regulator decoupling capacitor (typ. 0.22 μF) | 30 |
| SLEEP | Logic input for SLEEP mode | 31 |
| OSC | Logic-level oscillator (square wave) input | 32 |
| GND | Power and logic ground terminals | 33, 34, 35 |
| CP | Reservoir capacitor (typically 0.22 μF) | 36 |
| CP1 & CP2 | The charge pump capacitor (typically 0.22 μF) | 37 & 38 |
| NC | No (internal) connection | 39 |
| OUT _{1B} | DMOS H-bridge 1 – output B | 40 |
| NC | No (internal) connection | 41 |
| ENABLE ₁ | Logic input for bridge 1 – enable control | 42 |
| LOAD SUPPLY ₁ | V _{BB1} , the high current, 20 V to 50 V, supply for bridge 1 | 43 |
| GND | Power and logic ground terminals | 44 |

Package EB, 44-pin PLCC



For Reference Only
 (reference JEDEC MS-018 AC)
 Dimensions in millimeters
 Internally fused pins 44, 1 and 2; 11-13; 22-24; and 33-35
 Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
 Exact case and lead configuration at supplier discretion within limits shown
 ▲ Terminal #1 mark area

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